

DOWNLOAD WAFER LEVEL CHIP SCALE PACKAGING ANALOG AND POWER SEMICONDUCTOR APPLICATIONS

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SBVA017 NanoStar & NanoFree 300 m Solder Bump Wafer Chip-Scale Package Application 5 2 Physical Description 2.1 Package Characteristics The NanoStar package family is a Die Size BGA as identified by the JEDEC standards organiza-

NanoStar & NanoFree 300 m Solder Bump Wafer Chip-Scale

1, 1-trichloroethane; trichloroethate $1/f$, one over "f" noise where "f" is frequency 1D, one dimensional 1T-1C, 1 transistor/1 capacitor 1T-2C, 1 transistor/2 capacitor

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